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AT&T Bell Laboratories

subject: **AT&T OETC quarterly technical report for January-March 1993**

date: **April 13, 1993**

from: **J. L. Zilko**
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Enclosed please find copies of the Quarterly R & D Status and Technical Reports, including Financial Report, for ARPA Contract MDA972-92-C-0074 covering the period of January 1 through March 31, 1993.

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1. Overview of activities during Janauary-March 1993

The activities of January-March 1993 have continued to revolve around detailed design of the AT&T transmitter and receiver assemblies and associated pieceparts and in performing initial experiments to determine the feasibility of the design approach.

1.1 Task A.1: VCSEL fabrication

As described in the last quarterly report, a standard OETC VCSEL design has been decided upon. As part of our routine processing sequence, we have decided to process two OETC SEL wafers/month. One will be our "standard" design to be run with the intention of obtaining initial data on reproducibility and yield. The second wafer will be an experimental variation of the standard which is intended to allow the further optimization of epi layer design and processing.

The SEL design chosen to be the standard is one that had previously given what we considered to be the best combination of low threshold currents, low threshold voltages, and high powers. Six wafers - three of the standard design and three with simple variations from the standard design have been grown and processed and four have been tested. Unfortunately, the results from these wafers have been disappointing, with two of the experimental structures not lasing and one of the experimental structures and the standard structure giving lasers with high threshold currents and voltages and low output power. During this time, SEL's of a different design have been grown and fabricated using the same equipment for a separate program and have produced good SEL's. This suggests that although the design that we have chosen is capable of producing SEL's with good properties, this design may not be sufficiently robust to give a high yield of high quality SEL's. We are now in the process of evaluating the results of the first several wafers and anticipate deciding on what design changes to make shortly so that results can be obtained by late May. Note that any design changes that we make would involve the mirror design and should not affect the mode quality (single or multimode) of the resulting SEL's.

Initial experiments have begun to incorporate an output window passivation coating to the SEL's. This is likely to be critical as environmental protection for the long term reliability of these devices. The primary criteria for a suitable passivation coating are that the thickness and index of refraction be well controlled so that the optical properties are not degraded and that the coating be patternable. On the basis of these initial experiments, we have decided that our approach to passivation will be to use plasma-deposited SiO_2 which has the above properties and which has recently been developed for another program. Alternative coatings may have long term advantages. However, the patternability of these alternatives would have to be developed.

A single device SEL test set for cw LIV measurements has been built and software to run it written. This test set will now be extended through the use of a probe card to run arrays so that uniformity data on many arrays can be taken easily.

Milestone 5, Task A.1, Version I lasers produced, is complete.

1.2 Task A.2: Transmitter packaging

Initial experiments on angle polishing fiber arrays have been carried out. The polishing has gone well, with smooth, uniform fiber ends and no fiber chipping at a 45° angle. These experiments were carried out using fiber arrays which had the polyimid overcoating intact. However, in a package, light from the SEL (or to the receiver) is transmitted through the side of the fiber and thus, through any overcoating that is on the fiber. Because of concerns about the optical quality (transmission, index) of the polyimid, we have performed experiments on stripping of the overcoating after angle polishing is complete.

We have found that both wet chemicals and an O_2 plasma readily strip the polyimid. Unfortunately, these treatments also strip the polyimid on all sides of the fiber and also strips the epoxy that holds the fibers in the Si V-grooves, thus leaving the fiber unsupported. In addition, we have found these chemical treatments to be messy and somewhat difficult to clean. For these reasons, we intend to investigate the fabrication of the fiber connector part using bare fiber, in which the overcoating has already been stripped. Because the outside diameter is slightly reduced in this case, we will also have to make a minor change in the Si piecepart that captures the fibers.

Our intention is to evaporate a metal onto the ends of the angle polished fiber to eliminate transmission loss from the polished fiber end. Calculations indicate that the dependence of reflectivity on polarization for a 45° fiber mirror is rather small (~ 1.2%) for Au, is somewhat larger (~ 2.8%) for Ag, and is very large (~ 12%) for Al. For this reason, we plan to use Au as the metal mirror. However, we have concerns about the ruggedness of the Au coating on SiO_2. Typically the adhesion of Au on dielectrics is enhanced using various adhesion metals such as Ti. Unfortunately, these adhesion enhancing metals are expected to degrade the reflectivity of the mirror. We are presently performing experiments to evaluate the adhesion and reflectivity of a Au mirror with only a very thin layer of adhesion metal. The hope is that the thin layer is sufficiently transmissive so that only a minor degradation of optical properties occurs, but is sufficiently thick so as to promote adhesion. In the mean time, Au without any adhesion enhancing metals will be used so that its ruggedness can be evaluated.

We have had trials in epoxy mounting the monitor photodiodes onto the monitor SEL's from a mechanical wafer. There does not appear to be any problem with this attachment process. An assessment of the photocurrent response of the monitor photodiodes (nominally 0.5 A/W) will be done when good SEL chips become available.

The package design calls for the self-aligned solder attachment of the SEL chip to a Si submount. Although the initial package will not rely on self-alignment of the SEL chip (since three degrees of assembly freedom will be allowed for the first iteration package), we will explore self-alignment technology with the intention of relying on self-alignment for subsequent versions of the package. In order to do this, we have designed a solder scheme, including solder and solder dam mask opening requirements and solder thickness. We have recently received a mask so that bonding geometry and solder reflow conditions can be optimized.

The mechanical interface between the optical subassembly and the HIC into which the OSA will be packaged has been designed. The design had to accommodate the springs, clips, and other assembly hardware that are required to capture the MAC (TM) connector pins from the side while providing enough vertical force to hold the fiber connector together. This task was made somewhat more difficult because the Si submount and SEL chip are wider than the MAC (TM) connector, thus making a wraparound design difficult to fabricate. After considering a number of alternatives, we decided upon a rather simple design which allows the use of a modified MAC (TM) clip, a simple spring, and a plastic cover for the package, and which allows the direct heat sinking of the Si submount for the SEL to the heat spreader.

With the spring/clip arrangement decided upon, detailed drawings of the Si submount and heat spreader have been put together. In addition, a preliminary design of the layout of the poly/ceramic FIC has been completed. Bond pads on the side of the FIC that interfaces with the SEL chip (with 100 X 300 μm pads on 140 μm pitch) are staggered, have dimensions of 150 X 200 μm and have a 300 μm pitch. Since the SEL ground connection comes from the bottom of the SEL chip (top of the Si submount), the ground connection will be brought up to the top of the FIC through via holes in the ceramic. The other end of the traces remain undefined (as does the rest of the package) until additional information can be obtained concerning the driver chip. GE estimates this to be in mid to late May.

Milestone 5, Task A.2, Start package redesign, is complete.

1.3 Task A.3: Receiver packaging

A number of the items described in the transmitter section, section A.2, are applicable to the receiver. In particular, the work on angle polishing fibers, evaporated mirrors, and the mechanical interface between the OSA and the HIC are directly applicable to the receiver.

Optical crosstalk and coupling measurements were made on detector chips supplied by IBM using a 45° polished fiber and an 850 nm SEL source. Detectors had a 140 μm pitch and were round with 80 μm and 100 μm diameters. The data indicates that for the 100 μm detector, a 3% reduction in coupling and a constant -27 dB optical crosstalk exists in going from a fiber-detector separation of 0 μm to 100 μm while for the 80 μm detector there is a 6% reduction in coupling and an increase in crosstalk from -35 dB to -30 dB as the separation increases from 0 μm to 100 μm. This data has been communicated to IBM who will make the detector an 80 X 100 μm oval.

Based on estimates of the limits of wire bonding technology, we have requested that IBM provide a slight fanout of their bond pads from the 70 μm pitch that corresponds to the 140 μm fiber pitch to a 75 μm pitch. This increased pitch will allow much more robust wire bonding using state-of-the-art bonding equipment. The increased pitch will not result in an increase in chip size.

Detailed drawings have been put together for the receiver Si submount and heat spreader. In addition, a preliminary sketch of the layout of the poly/ceramic FIC has been completed. Bond pads on the side of the FIC that interfaces with the receive chip are envisioned to be 45 X 100 μm and have a 75 μm pitch to match the bond pads on the receiver chip. The two sides of the FIC that surround the sides of the receiver chip carry power and ground traces and have decoupling capacitors.

Milestone 4, Task A.3, Start Package Redesign, is complete.

1.4 Task A.4: Fiber connector

The first prototype jumper cable and 8 additional fiber jumper cables have been fabricated. They were terminated on each end with panel mount-cable end hardware The connector loss was as expected: an average of 0.58 dB with a standard deviation of 0.25 dB. The 8 additional models were made with a variety of lengths so that the testbed can explore both long (dispersion and skew) and short (model noise due to unfilled modes in the fiber) limits to the interconnect length. The lengths chosen were 0.3 m, 0.5 m, 1 m, 2 m, 3 m, 5 m, 10 m, and 50 m.

Milestone 3, Task A.4, First model, which had not been completed at the last quarterly report, has now been completed.

Milestone 4, Task A.4, Eight more cables fabricated, has been completed.

1.5 Task A.5: Project Management

Considerable time and effort has been spent in monitoring progress on this program and coordinating the efforts both within AT&T and between AT&T, IBM, GE, and Honeywell. Numerous interactions via e-mail, telephone, and FAX were held among the OETC member companies. In addition, one intercompany meeting was held at AT&T, Murray Hill, New Jersey to discuss OETC technical issues.

2. Anticipated activity for April-June 1993

2.1 Task A.1: VCSEL fabrication

It is anticipated that the standard SEL design will be reevaluated, new wafers grown and processed, and results from a redesign will be available.

2.2 Task A.2: Transmitter packaging

It is anticipated that Si optical bench pieceparts will be fabricated and assembled into mechanical optical subassemblies and that the HIC design will be complete.

Because the GE driver chips will not be ready for a design review until mid to late May and have an 8 week fabrication interval, we anticipate that the scheduled first delivery of a transmitter module, Milestone 8, Task A.8, Deliver mechanical models, Version I, will be missed.

2.3 Task A.3: Receiver package

It is anticipated that Si optical bench pieceparts will be fabricated and that the HIC design will be complete.

Because the IBM receiver chip design will not be completed until early April and chips will not be available until late July, we anticipate that the scheduled first delivery of a receiver module, Milestone 5, Task A.3, Deliver mechanical models, Version I, will be missed.

2.4 Task A.4: Fiber connector

It is anticipated that an additional 8 connectorized 32 fiber jumper cables will have been fabricated.